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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/997,228	11/29/2001	Daniel M. Joffe	72129	2539

27975 7590 01/11/2006

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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/997,228	JOFFE ET AL.	
	Examiner	Art Unit	
	Walter F. Briney III	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. **Claims 6 and 9-16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.**

Claim 11 recites that the output impedance of said synthetic impedance driver circuit is synthesized in terms of the mirror current ratio k supplied by an output current-dependent current source, the value of an output voltage feedback resistor and, in accordance with the current amendments, the feedback from an output voltage feedback device. Therefore, no less than three separate sources are being used in deriving the synthetic output impedance. In contrast to the applicant's specification no more than two sources are ever used in generating feedback currents used in synthesizing an output impedance. Figures 5-8 clearly indicate this fact. For example, figure 8 includes a circuit comprising elements (81), (91), (100), (110), (120), (130) and (140) that can be regarded as either an output current-dependent current source or a current mirror circuit and a feedback resistor (55). However, there is no disclosure of three sources simultaneously affecting the synthetic output impedance, and the newly presented claim recitations discussed above constitute new matter. For the purposes of

this action, it is assumed that the output voltage feedback device corresponds to the voltage feedback resistor as claimed.

Claims 12-16 are dependent on claim 11, thus incorporating the limitations of claim 11, and are rejected for the same reasons.

Claims 6, 9 and 10 recite *an output voltage feedback resistor* in addition to the output voltage feedback device of claim 1. As noted above apropos claim 11, only two feedback paths exist. One is a voltage feedback path and the second a current feedback path. The applicant has essentially claimed two voltage feedback paths and a current feedback path. For the purposes of this action, it is assumed that the output voltage feedback device and the output voltage feedback resistor are the same.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claim 16 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

Claim 16 recites *said current mirror node*, in line 4 of the claim. As claim 16 depends from both claims 11 and 13, it follows that claim 16 inherits the limitations of those claims, resulting in an ambiguity as to which current mirror node the claim is referring to. Claim 11 generally recites a current mirror node in line 22 while claim 13 specifically defines a current mirror node in line 9. For the purposes of this action, claim 16 is assumed to be referring to the current mirror node of claim 13. Appropriate correction is required.

Assuming for the sake of argument that *said current mirror node* is referring to the current mirror node defined according to claim 13 and that the feedback resistor and feedback device defined according to claim 11 are the same, claim 16 is allowable over Navabi. In particular, the current mirror node of claim 13 is defined as a single node that provides feedback current under the control of two complementary transistors. In contrast, Navabi discloses a current mirror node as a node that supplies feedback current under the control of one supply transistor 345 and one error transistor 346.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1 and 4-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Navabi et al. (US Patent 5,585,763).**

Claim 1 is limited to *a synthetic impedance driver circuit for driving a load.* Navabi discloses a controlled impedance amplifier (i.e. *a synthetic impedance driver circuit for driving a load*) (abstract). Navabi discloses *an input port* (figure 2, element 325) *adapted to receive an input signal* (figure 2, element i_{in}) *to be coupled to said load* (figure 2, element R_L). Navabi discloses *an output port* (figure 2, element 360) *adapted to apply an output signal* (figure 2, element V_{out}) *to said load* (figure 2, element R_L), the output port clearly defining *an output current node.* Navabi discloses *an operational*

amplifier (figure 2, element 310) *having an input* (figure 2, positive terminal of 310) *coupled to said input port* (figure 2, element 325) *and a single output*. Navabi discloses that the operational amplifier drives output amplifiers 347 and 357 (i.e. *coupled to said output port*) and drives feedback transistors 345 and 355 (i.e. *over a circuit path through which an output impedance of said driver circuit is synthesized*). The feedback resistor R_f is not a part of the output or transistor feedback path (i.e. *said circuit path being exclusive of one or more series coupled electrical energy-dissipative elements*). Thus, Navabi inherently discloses *that said synthesized output impedance of said driver circuit is defined essentially exclusive of series-coupled electrical energy-dissipative elements.* The previously mentioned feedback resistor R_f 366 corresponds to *an output voltage feedback device* and transistors 346 and 356 correspond, at least in part, to the *current mirror circuit* as claimed. As the outputs of the amplifier 310 are commonly applied to both transistors 345 and 347 as well as transistors 355 and 357, it is inherent that the current returned to the amplifier 310 from transistors 346 and 356 is representative of the output current applied to the output port by transistors 347 and 357. The current mirror circuit defined by transistors 346 and 356 includes two drain nodes or *current mirror nodes*, each tracking a portion of output voltage applied to the output node by one of transistors 347 and 357. In addition, two error amplifiers 370 and 375 respectively adjust the voltage at the output of transistors 345 and 347 to more closely reflect that at the output node, which corresponds to *removing current mirror distortion for values of load resistance*. See column 5, line 66, through column 6, line 2. The error amplifiers include two inputs, one of which couples to the output node and the

other of which couples to the current mirror node of either transistor 345 or transistor 355. Furthermore, the error amplifiers have outputs connected to the control terminals of transistors 346 and 356, which also compose part of the *current mirror circuit* as recited. In this way, the error amplifiers 370 and 375 correspond to *feedback amplifiers.* Therefore, Navabi anticipates all limitations of the claim.

Claim 4 is limited to *the synthetic impedance driver circuit according to claim 2*, as covered by Navabi. Navabi discloses an operational amplifier (figure 2, element 310) that performs a level-shifting function with two outputs (figure 2, elements 315, 320). Navabi discloses *an output coupling circuit* (figure 2, elements 345, 355, 347, 357) *having an input coupled to said output of said operational amplifier and level-shifted outputs.* Navabi discloses complementary output transistors 347 and 357 that are *respectively coupled between said level-shifted outputs of said output coupling circuit and said output port.* Navabi discloses *complementary polarity current mirror transistor circuits* (figure 2, elements 345, 355) *respectively coupled between said complementary polarity output transistor circuits and an input of said operational amplifier.* Therefore, Navabi anticipates all limitations of the claim.

Claim 5 is limited to *the synthetic impedance driver circuit according to claim 4*, as covered by Navabi. Navabi discloses an operational amplifier (figure 2, element 310) that performs a level shift with a plurality of output levels (i.e. *wherein said output coupling circuit includes a level shifter*) (figure 2, element 315, 320). Therefore, Navabi anticipates all limitations of the claim.

Claim 6 is limited to *the synthetic impedance driver circuit according to claim 5*, as covered by Navabi. Navabi discloses an *operational amplifier that has a first polarity input* (figure 2, positive terminal of 310) *to which said input signal* (figure 2, element i_{in}) *and an output voltage feedback device are coupled* (figure 2, element R_f), *and a second polarity input* (figure 2, negative terminal of 310) *to which a reference voltage is coupled* (figure 2, element V_{cm}). Therefore, Navabi anticipates all limitations of the claim.

Claim 7 is limited to *the synthetic impedance driver circuit according to claim 6*, as covered by Navabi. Navabi discloses a x-intersection where lines 343, 353 and 325 cross (i.e. *wherein said complementary polarity current mirror circuits have a first common node coupled to said first polarity input of said operational amplifier*). Therefore, Navabi anticipates all limitations of the claim.

Claim 8 is limited to *the synthetic impedance driver circuit according to claim 7*, as covered by Navabi. Navabi discloses a x-intersection where lines 344, 352, and 360 cross (i.e. *wherein said complementary polarity output transistor circuits have a second common node coupled to said output port*). Therefore, Navabi anticipates all limitations of the claim.

Claim 9 is essentially the same as claim 6 and is rejected for the same reasons.

Claim 10 is limited to *the synthetic impedance driver circuit according to claim 2*, as covered by Navabi. Navabi discloses a second embodiment that adds a switching input to the operational amplifier (figure 8A). It is clear that this embodiment incorporates all the limitations of claim 2. In addition, Navabi discloses that *said operational amplifier circuit* (figure 8A, element 910) *has a first polarity input* (figure 8A,

IN1+ terminal of 910) *to which said input signal is coupled* (figure 8A, i_{in}), *and a second polarity input* (figure 8A, IN2+ terminal of 910) *to which an output voltage feedback device and said feed back current are coupled.* Therefore, Navabi anticipates all limitations of the claim.

Claim 11 is limited to *a synthetic impedance driver circuit.* Navabi discloses a controlled impedance amplifier (i.e. *a synthetic impedance driver circuit*) (abstract). Navabi discloses *an operational amplifier* (figure 2, element 310) *having a first input* (figure 2, positive terminal of 310) *coupled to receive an input signal* (figure 2, element i_{in}), *a second input* (figure 2, negative terminal of 310) *coupled to a reference voltage* (figure 2, element V_{cm}), *and a voltage feedback resistor* (figure 2, element R_f) *coupled between an output port and an input of said amplifier*, the driver also comprising *an output port* 360 *adapted to supply an output signal to a load* R_L, the output port inherently including *an output current node.* Navabi discloses *an output current-dependent current source* (figure 2, elements 345, 355). These devices are biased by devices 346 and 356 to inherently supply *a prescribed fraction k of output current at said output port over a current feedback path to an input of said operational amplifier.* Because all elements are disclosed by Navabi, Navabi inherently discloses *that the output impedance of said synthetic impedance driver circuit is synthesized in terms of the mirror current ratio k and the value of said output voltage feedback resistor.* The operational amplifier has a *single* differential *output* as seen in figure 2A. As explained in the previous section entitled "Claim Rejections - 35 USC § 112," the output voltage feedback device and resistor are equivalent. In view of this, the new limitations recited

in this claim are essentially the same as those newly presented in claim 1, and are rejected for the same reasons. Therefore, Navabi anticipates all limitations of the claim.

Claim 12 is limited to *the synthetic impedance driver circuit according to claim 11*, as covered by Navabi. Navabi discloses that the operational amplifier (figure 2, element 310) has a feedback path through devices 345 and 355, and that the *output* is generated by elements 347 and 357, therefore, *no energy dissipative devices* are present in the output. Also, the current feedback by elements 345 and 355 *is free of dissipative elements*. Therefore, Navabi anticipates all limitations of the claim.

Claim 13 is limited to *the synthetic impedance driver circuit according to claim 12*, as covered by Navabi. Navabi discloses an operational amplifier (figure 2, element 310) that performs level shifting to properly control all output transistors (i.e. *said output coupling circuit including a level shifter*). The shifter has *a first* (figure 2, element 315) *and second* (figure 2, element 320) *level-shifted outputs, respectively coupled to first* (figure 2, element 347) *and second* (figure 2, element 357) *complementary polarity output transistors coupled to said output port, and associated complementary current mirror transistors* (figure 2, elements 345, 355) having *a node* at the intersection of lines 343, 353 and 325. Because 345 and 355 are further controlled by 346 and 356, they inherently provide *said prescribed fraction k of output current at said output port to an input of said operational amplifier*. Therefore, Navabi anticipates all limitations of the claim.

Claim 14 is limited to *the synthetic impedance driver circuit according to claim 12*, as covered by Navabi. Navabi discloses *an input signal* (figure 2, element i_{in}) *is*

coupled to a noninverting input (figure 2, positive terminal of 310) *of said operational amplifier*. Therefore, Navabi anticipates all limitations of the claim.

Claim 15 is limited to *the synthetic impedance driver circuit according to claim 13*, as covered by Navabi. Navabi discloses a feedback path including several resistors (figure 8, elements Rf1, Rf2) coupled to a mirror current feedback (figure 8, elements output from 347 and 357). One of these resistors is the resistive feedback from the output. The other is *a first auxiliary resistor*. Navabi also discloses that a third resistor (i.e. *a second auxiliary resistor*) is used (column 8, lines 32-35). The resistors are shown as being feedback to *non-inverting reference inputs of the amplifier* (figure 8, element 910). Therefore, Navabi anticipates all limitations of the claim.

Claim 16 is limited to *the synthetic impedance driver circuit according to claim 13*, as covered by Navabi. Navabi discloses *a feedback operational amplifier* (figure 7, element 370) *having inputs respectively coupled to said output port* (figure 7, element 342) *and to a current mirror node* defined by arrow 341. Assuming for the sake of argument that *said current mirror node* is referring to the current mirror node defined according to claim 13, claim 16 is allowable over Navabi. In particular, the current mirror node of claim 13 is defined as a single node that provides feedback current under the control of two complementary transistors. In contrast, Navabi discloses a current mirror node as a node that supplies feedback current under the control of one supply transistor 345 and one error transistor 346. Thus, claim 16 would be allowable over Navabi after overcoming the rejections under 35 U.S.C. § 112, second paragraph.

Response to Arguments

Applicant's arguments filed 17 October 2005 have been fully considered but they are not persuasive.

In contrast to the applicant's remarks on pages 8 and 9 of the current response, Navabi clearly discloses the use of a second amplifier 370 that meets the claim limitations as set forth in the preceding sections.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F. Briney III whose telephone number is 571-272-7513. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SINH TRAN
SUPERVISORY PATENT EXAMINER

WFB